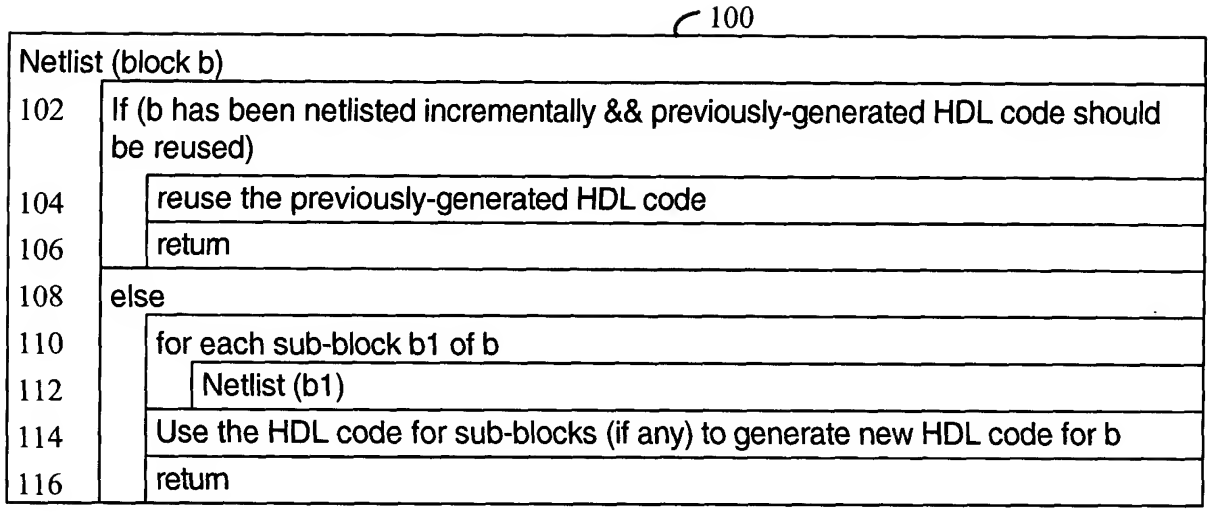
100
Netlist (block b)
102
If (b has been netlisted incrementally && previously-generated HDL code should be reused)
104
reuse the previously-generated HDL code
106
return
108
else
110
for each sub-block b1 of b
112
Netlist (b1)
114
Use the HDL code for sub-blocks (if any) to generate new HDL code for b
116
return

FIG. 1

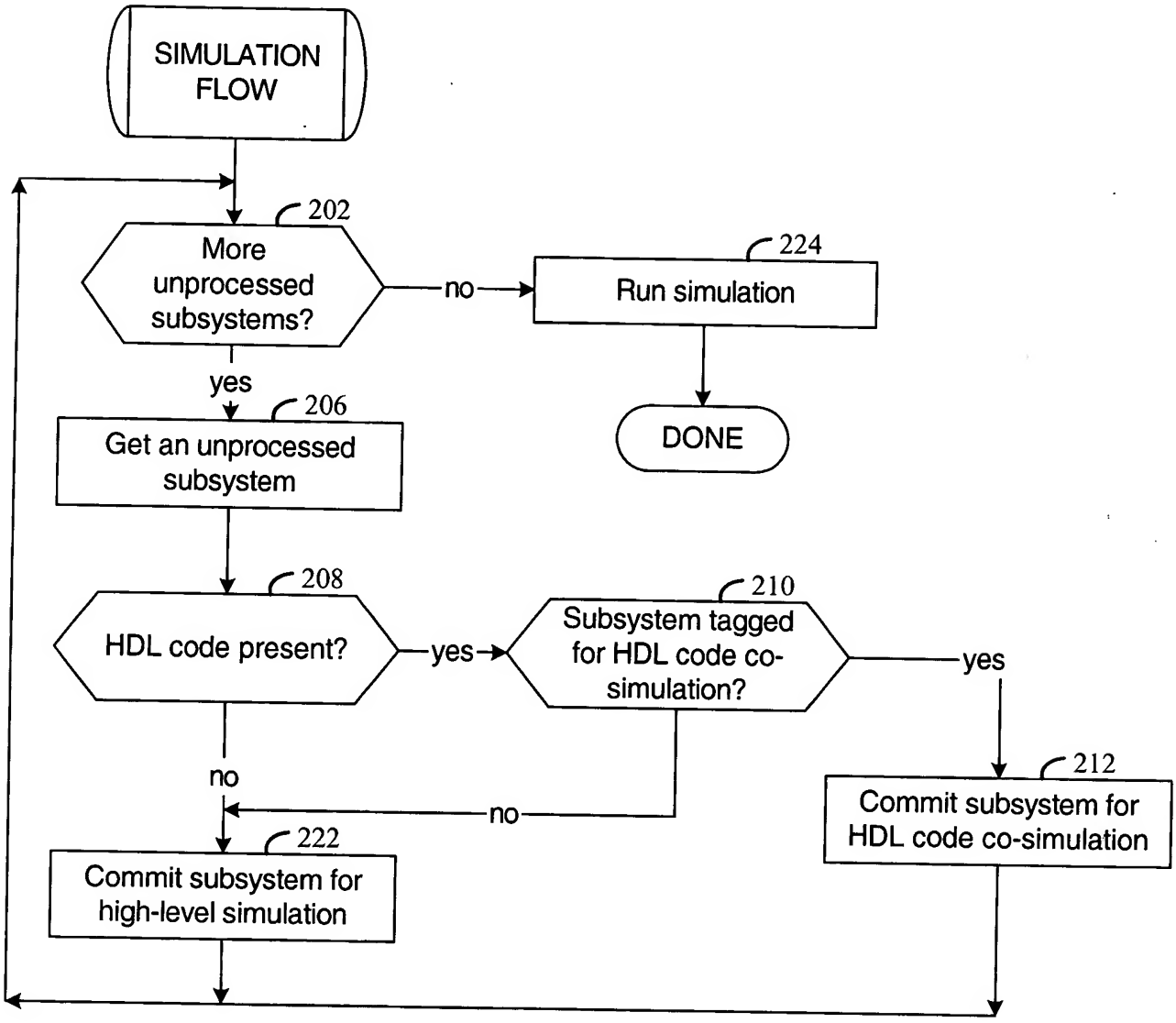
SIMULATION FLOW
202
More unprocessed subsystems?
no
224
Run simulation
DONE
yes
206
Get an unprocessed subsystem
208
HDL code present?
yes
210
Subsystem tagged for HDL code co-simulation?
yes
212
Commit subsystem for HDL code co-simulation
no
no
222
Commit subsystem for high-level simulation

FIG. 2

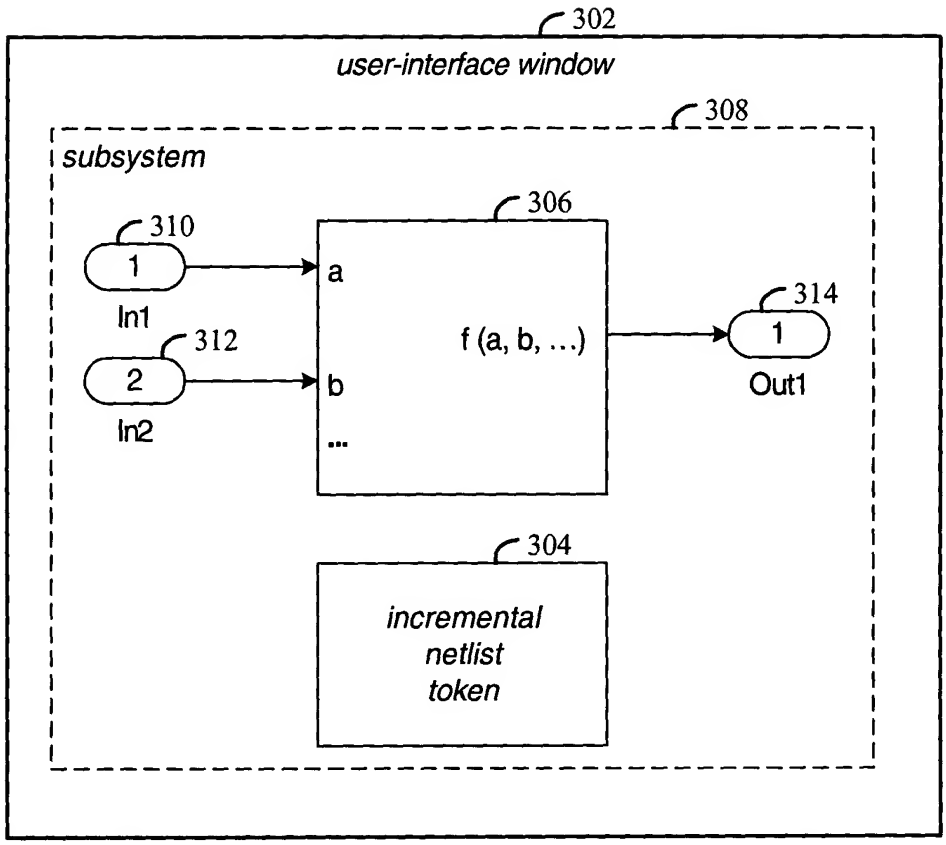
302
user-interface window
308
subsystem
306
310
1
In1
a
312
2
In2
b
...
f (a, b, ...)
314
1
Out1
304
incremental
netlist
token

FIG. 3

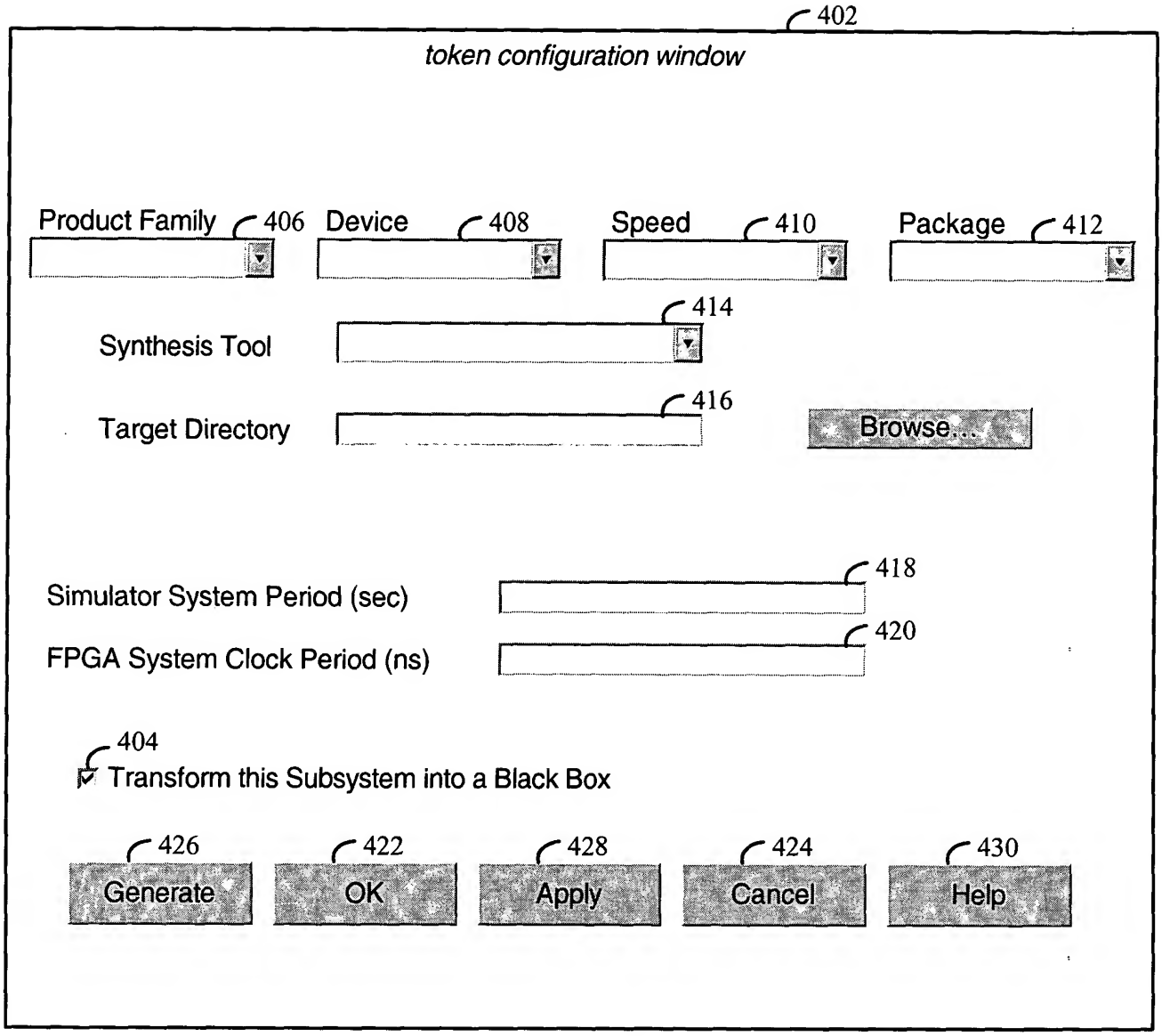
402
token configuration window
Product Family
406
Device
408
Speed
410
Package
412
414
Synthesis Tool
416
Target Directory
Browse...
418
Simulator System Period (sec)
420
FPGA System Clock Period (ns)
404
Transform this Subsystem into a Black Box
426
422
428
424
430
Generate
OK
Apply
Cancel
Help

FIG. 4

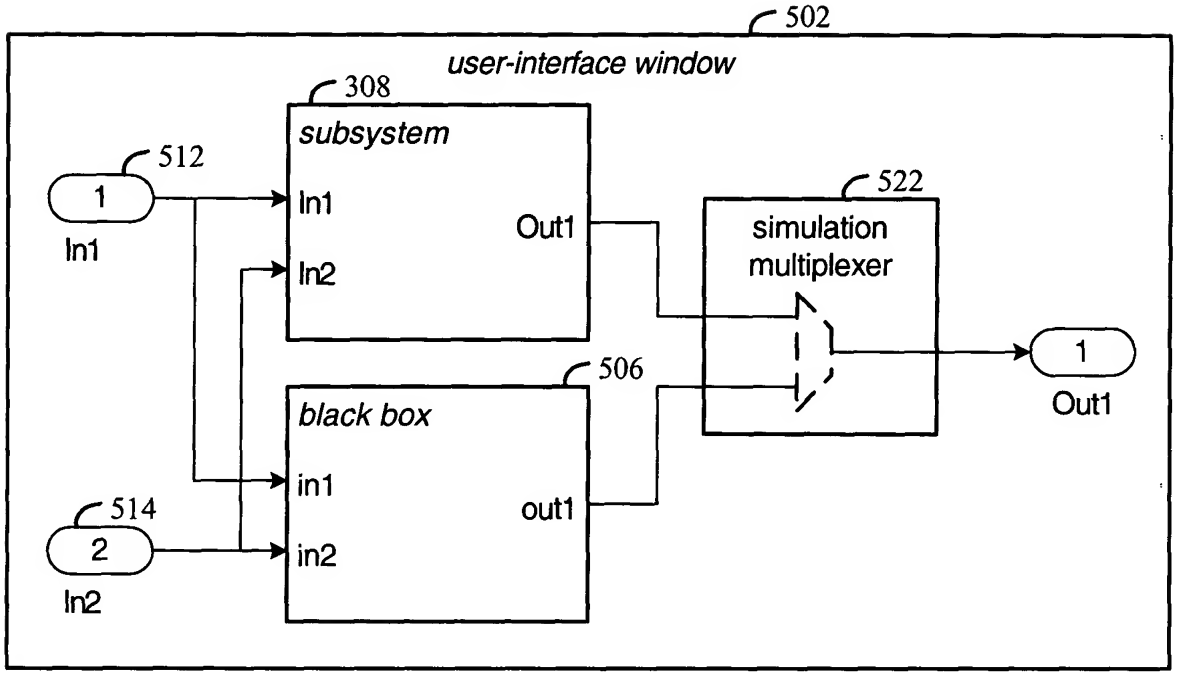
502
user-interface window
308
subsystem
512
1
In1
In1
In2
Out1
522
simulation
multiplexer
1
Out1
506
black box
in1
out1
514
2
In2
in2

FIG. 5

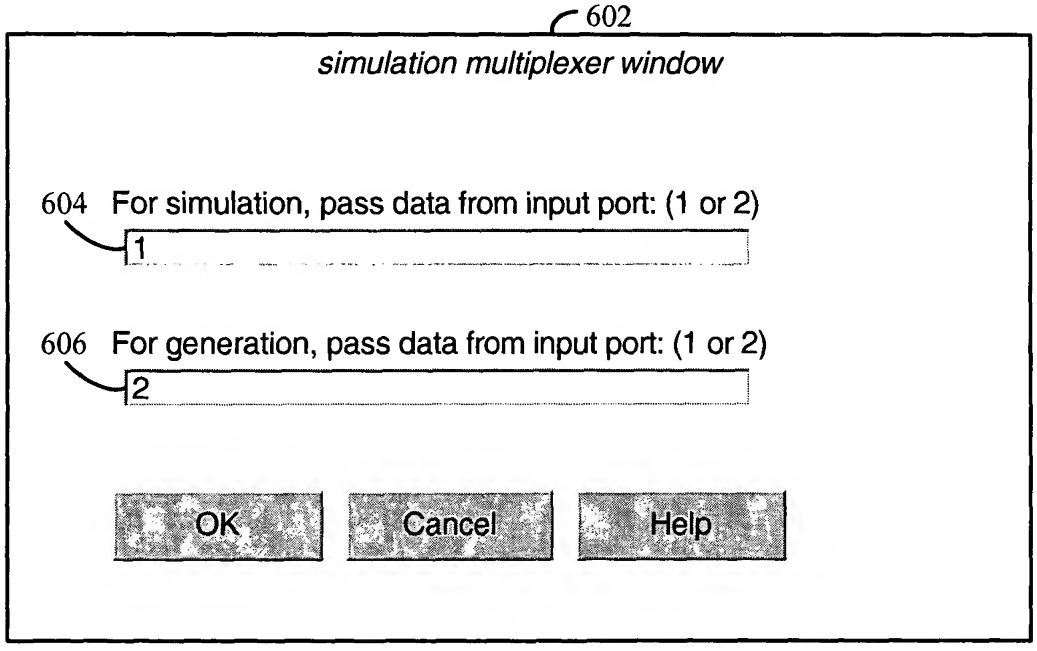
602
simulation multiplexer window
604 For simulation, pass data from input port: (1 or 2)
1
606 For generation, pass data from input port: (1 or 2)
2
OK
Cancel
Help

FIG. 6